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1 [New perspectives in physical design: Uncertainty-aware circuit optimization](#)


Xiaoliang Bai, Chandu Visweswariah, Philip N. Strenski

 June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(131.43 KB)

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Almost by definition, well-tuned digital circuits have a large number of equally critical paths, which form a so-called "wall" in the slack histogram. However, by the time the design has been through manufacturing, many uncertainties cause these carefully aligned delays to spread out. Inaccuracies in parasitic predictions, clock slew, model-to-hardware correlation, static timing assumptions and manufacturing variations all cause the performance to vary from prediction. Simple statistical princip ...

Keywords: circuit tuning, nonlinear, optimization, performance optimization, process variation, small uncertainty, transistor sizing

2 [Block-based Static Timing Analysis with Uncertainty](#)


Anirudh Devgan, Chandramouli Kashyap

 November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(181.39 KB)

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Static timing analysis is a critical step in design of any digitalintegrated circuit. Technology and design trends have ledto significant increase in environmental and process variationswhich need to be incorporated in static timing analysis.This paper presents a new, efficient and accurate block-basedstatic timing analysis technique considering uncertainty.This new method is more efficient as its modelsarrival times as cumulative density functions (CDFs) anddelays as probability functions (PDFs ...

3 [Design automation methodology and rf/analog modeling for rf CMOS and SiGe BiCMOS technologies](#)


D. L. Hareme, K. M. Newton, R. Singh, S. L. Sweeney, S. E. Strang, J. B. Johnson, S. M. Parker, C. E. Dickey, M. Erturk, G. J. Schulberg, D. L. Jordan, D. C. Sheridan, M. P. Keene, J. Boquet, R. A. Groves, M. Kumar, D. A. Herman, B. S. Meyerson

 March 2003 **IBM Journal of Research and Development**, Volume 47 Issue 2-3

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The rapidly expanding telecommunications market has led to a need for advanced rf

integrated circuits. Complex rf- and mixed-signal system-on-chip designs require accurate prediction early in the design schedule, and time-to-market pressures dictate that design iterations be kept to a minimum. Signal integrity is seen as a key issue in typical applications, requiring very accurate interconnect transmission-line modeling and RLC extraction of parasitic effects. To enable this, IBM has in place ...

4 Low-power circuits and technology for wireless digital systems

S. V. Kosonocky, A. J. Bhavnagarwala, K. Chin, G. D. Gristede, A.-M. Haen, W. Hwang, M. B. Ketchen, S. Kim, D. R. Knebel, K. W. Warren, V. Zyuban

March 2003 **IBM Journal of Research and Development**, Volume 47 Issue 2-3

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As CMOS technology scales to deep-submicron dimensions, designers face new challenges in determining the proper balance between aggressive high-performance transistors and lower-performance transistors to optimize system power and performance for a given application. Determining this balance is crucial for battery-powered handheld devices in which transistor leakage and active power limit the available system performance. This paper explores these questions and describes circuit techniques fo ...

5 Coping with variability: the end of deterministic design: Death, taxes and failing chips

Chandu Visweswariah.

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available:  pdf(145.71 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In the way they cope with variability, present-day methodologies are onerous, pessimistic and risky, all at the same time! Dealing with variability is an increasingly important aspect of high-performance digital integrated circuit design, and indispensable for first-time-right hardware and cutting-edge performance. This invited paper discusses the methodology, analysis, synthesis and modeling aspects of this problem. These aspects of the problem are compared and contrasted in the ASIC and custom ...

Keywords: Statistical timing, design methodology, parametric yield prediction

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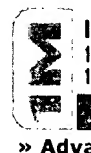
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Spangler, A.;

Potentials, IEEE , Volume: 15 , Issue: 4 , Oct.-Nov. 1996

Pages:29 - 32

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2 Exploitation of Hierarchy in Analyses of Integrated Circuit Artwork
Newell, M.E.; Fitzpatrick, D.T.;

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Pages:192 - 200

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Macii, E.; Plessier, B.; Somenzi, F.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 16 , Issue: 10 , Oct. 1997

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[\[Abstract\]](#) [\[PDF Full-Text \(804 KB\)\]](#) **IEEE JNL**
4 Matching in the presence of don't cares and redundant sequential elements for sequential equivalence checking
Rahim, S.; Rouzeyre, B.; Torres, L.; Rampon, J.;

High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International , 12-14 Nov. 2003

Pages:129 - 134

[\[Abstract\]](#) [\[PDF Full-Text \(378 KB\)\]](#) IEEE CNF

5 Redundant functional faults reduction by saboteurs synthesis [logic verification]

Fummi, F.; Marconcini, C.; Pravadelli, G.;

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Pages:108 - 113

[\[Abstract\]](#) [\[PDF Full-Text \(432 KB\)\]](#) IEEE CNF

6 General framework for removal of clock network pessimism

Zejda, J.; Frain, P.;

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Pages:632 - 639

[\[Abstract\]](#) [\[PDF Full-Text \(603 KB\)\]](#) IEEE CNF

7 Emulation-based design errors identification

Castelnuovo, A.; Fin, A.; Fummi, F.; Sforza, F.;

Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 17 IEEE International Symposium on , 6-8 Nov. 2002

Pages:365 - 371

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8 Design for verification at the register transfer level

Ghosh, I.; Sekar, K.; Boppana, V.;

Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia South Pacific and the 15th International Conference on VLSI Design. Proceedings , 7-11 Jan. 2002

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9 Constraints specification at higher levels of abstraction

Balarin, F.; Burch, J.; Lavagno, L.; Watanabe, Y.; Passerone, R.; Sangiovanni Vincentelli, A.;

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10 Estimation of aperture response functions from measurements using non-ideal detector

Clinthorne, N.H.; Wrobel, M.C.; Ng, C.; Rogers, W.L.;

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Pages:958 - 962 vol.2

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 Design, Automation and Test in Europe Conference and Exhibition 2000.
 Proceedings, 27-30 March 2000/
 Pages:396 - 401

[\[Abstract\]](#) [\[PDF Full-Text \(40 KB\)\]](#) **IEEE CNF**
2 Proceedings International Test Conference 2000 (IEEE Cat. No.00CH37159)

Test Conference, 2000. Proceedings. International, 3-5 Oct. 2000

[\[Abstract\]](#) [\[PDF Full-Text \(544 KB\)\]](#) **IEEE CNF**
3 RTL-based functional test generation for high defects coverage in di SOCs*Santos, M.B.; Goncalves, F.M.; Teixeira, I.C.; Teixeira, J.P.;*
 European Test Workshop, 2000. Proceedings. IEEE, 23-26 May 2000
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5 Validating fault tolerant designs using laser fault injection (LFI)*Samson, J.R., Jr; Moreno, W.; Falquez, F.;*

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6 A method for the evaluation of behavioral fault models

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High-Level Design Validation and Test Workshop, 2003. Eighth IEEE
International , 12-14 Nov. 2003
Pages:169 - 172

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Soden, J.M.; Hawkins, C.F.;
Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995 ,
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13 A methodology for rapid prototyping of real-time image processing systems

Kralijic, I.C.; Quenot, G.M.; Zavidovique, B.;

Rapid System Prototyping, 1995. Proceedings., Sixth IEEE International Workshop, 7-9 June 1995

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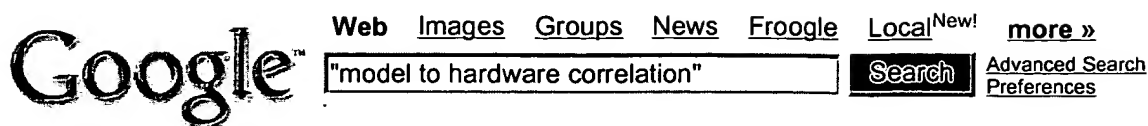
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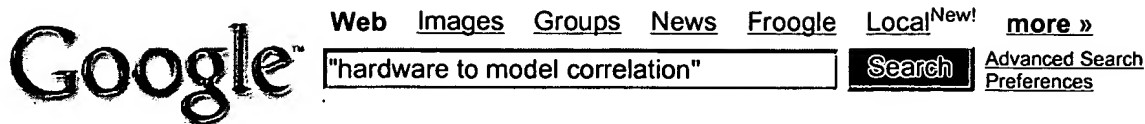
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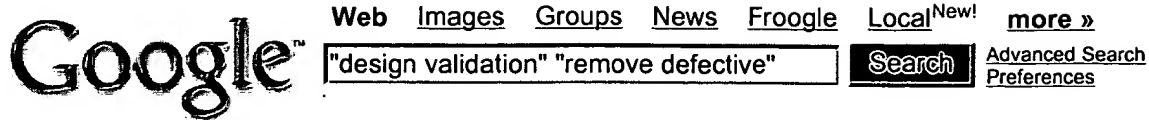
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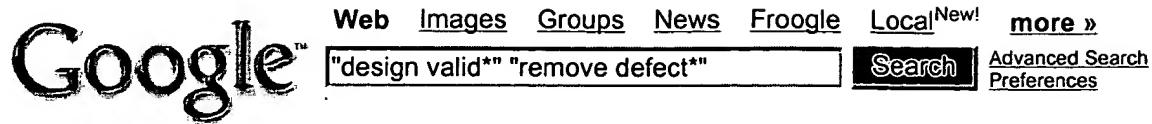
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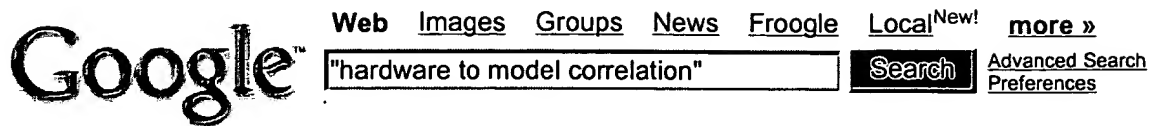
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